What is claimed is:

1. An integrated circuit, comprising:

a semiconductor substrate comprising device elements and one or more metallization layers interconnecting the device elements and having an uppermost layer;

a protective overcoat formed over the metallization layers, the protective overcoat having vias through it;

tungsten plugs substantially filling the vias and connecting to the uppermost layer; and

thick copper formed over the protective overcoat and forming connections to the tungsten plugs.

2. The integrated circuit of claim 1, wherein the uppermost layer is an aluminum metallization layer.

3. The integrated circuit of claim 1, wherein the protective overcoat comprises one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers and silicon nitride layers.

4. The integrated circuit of claim 1, wherein the vias have a critical dimension of about 2 μm or less.

5. The integrated circuit of claim 4, further comprising larger vias having a critical dimension of about 5 μm or greater, wherein tungsten forms a layer within the larger vias.

6. The integrated circuit of claim 1, wherein the vias have a critical dimension of about 1.0 μm or less.

7. The integrated circuit of claim 1, wherein the thick copper forms interconnections between device elements within the integrated circuit.

8. A method of manufacturing an integrated circuit, comprising:

forming a semiconductor substrate comprising device elements;

forming one or more metallization layers over the device elements, the one or more metallization layers interconnecting the device elements and having an uppermost layer;

forming a protective overcoat layer over the uppermost layer;

patterning vias through the protective overcoat layer to selectively expose the uppermost metallization layer;

substantially filling the vias with a metal having a coefficient of thermal expansion less than or equal to about 8 ppm/°C to form metal plugs;

forming a seed layer over the substrate;

forming a patterned resist coating over the seed layer, wherein the pattern exposes the seed layer over the metal plugs;

plating from the seed layer to form thick copper connections to the metal plugs.

9. The method of claim 8, wherein the vias are patterned with an anisotropic dry etch process, whereby the vias have steep walls.

10. The method of claim 8 wherein the thick copper connections comprise interconnections between device elements within the integrated circuit.

11. The method of claim 8 wherein the uppermost metallization layer is an aluminum metal layer.

12. The method of claim 8, wherein the metal is tungsten.

13. The method of claim 8, wherein the vias have critical dimensions of about 2 μm or less.

14. The method of claim 13, wherein patterning further comprises patterning larger vias having critical dimensions of about 5 μm or greater.

15. The method of claim 8, wherein the protective overcoat comprises one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers and silicon nitride layers.

16. An integrated circuit, comprising:

a semiconductor substrate comprising device elements and one or more metallization layers interconnecting the device elements, the one or more metallization layers having an uppermost layer, the uppermost layer comprising bond pads;

a protective overcoat formed over the metal layers, the protective overcoat having vias through it, wherein arrays of vias are formed over individual bond pads;

metal plugs substantially filling the vias and connecting to the bond pads; and

thick copper connections to the metal plugs.

17. The integrated circuit of claim 16, wherein the metal plugs are copper plugs.

18. The integrated circuit of claim 16, wherein the vias have a critical dimension of about 2 μm or less.

19. The integrated circuit of claim 16, wherein the metal plugs have a coefficient of thermal expansion less than or equal to about 8 ppm/°C.

20. The integrated circuit of claim 16, wherein the metal plugs are tungsten plugs.

21. The integrated circuit of claim 16, wherein the uppermost layer is an aluminum metallization layer.

22. The integrated circuit of claim 16, wherein the protective overcoat comprises one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers and silicon nitride layers.

23. The integrated circuit of claim 16, wherein the thick copper connections comprise interconnections between device elements within the integrated circuit.

24. A method of forming copper connectors on a semiconductor device comprising:

forming a semiconductor substrate comprising device elements;

forming one or more metallization layers over the devices elements, the one or more metallization layers interconnecting the device elements and having an uppermost layer that is a copper metallization layer;

forming a protective overcoat layer;

patterning the protective overcoat layer to form vias having a critical dimension of 2.0 μm or less across;

substantially filling the vias with a metal to form metal plugs;

electroplating thick copper connections to the metal plugs.

25. The method of claim 24, wherein the metal is copper.

26. The method of claim 25, wherein the metal is formed in the vias and overlies the protective overcoat, further comprising using the copper metal overlying the protective overcoat as a seed layer for the electroplating of the thick copper connections.

27. The method of claim 24, wherein the metal is tungsten.

28. The method of claim 24, wherein the metal has a coefficient of thermal expansion less than or equal to about 8 ppm/°C.

29. The method of claim 24, wherein the thick copper connections comprise interconnections between device elements within the integrated circuit.

30. An integrated circuit, comprising:

a semiconductor substrate comprising device elements and one or more aluminum metal layers interconnecting the device elements, the one or more aluminum metal layers having an uppermost layer;

a protective overcoat formed over the metal layers, the protective overcoat having vias through it;

metal plugs filling the vias and connecting to the uppermost layer; and

thick copper connections to the metal plugs;

wherein the thick copper connections comprise interconnections between device elements within the integrated circuit.

31. The integrated circuit of claim 30, wherein the metal plugs are formed of a metal having a coefficient of thermal expansion less than or equal to about 8 ppm/°C.

32. The integrated circuit of claim 30, wherein the metal plugs are formed of tungsten.